WE CLAIM:

1. A semiconductor integrated circuit device comprising a plurality of oscillators each having an oscillation node,

wherein said oscillation nodes of each of said oscillators are connected together.

2. A semiconductor integrated circuit device according to claim 1, wherein said oscillators are synchronized to oscillate with a substantially identical frequency at each of said oscillation nodes.

3. A semiconductor integrated circuit device according to claim 2, wherein said oscillators are synchronized to oscillate with a substantially identical phase at each of said oscillation nodes.

4. A semiconductor integrated circuit device according to claim 1, further comprising a conductive wiring line, wherein said oscillation nodes of each of said oscillators are connected together by said conductive wiring line.

5. A semiconductor integrated circuit device according to claim 4, wherein said conductive wiring line is formed in a shape of a closed loop.

6. A semiconductor integrated circuit device according to claim 4, wherein said conductive wiring line is formed in a shape of a mesh, and said oscillation nodes of said oscillators are connected at intersection points of said mesh.

7. A semiconductor integrated circuit device according to claim 4, wherein said oscillation nodes are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said connection points, wherein said interval lengths are substantially equal.

8. A semiconductor integrated circuit device according to claim 4, wherein said oscillation nodes are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said

connection points, wherein said interval of length is at least 50 μm.

9. A semiconductor integrated circuit device according to claim 1, wherein said oscillators are ring oscillation circuits.

10. A semiconductor integrated circuit device according to claim 1, wherein said oscillators are delay lines having multistage connected inverters.

11. A semiconductor integrated circuit device, comprising:

a plurality of ring oscillation circuits having inverters connected in a ring shape; and

a conductive wiring line,

wherein an output of at least one inverter of each said ring oscillation circuit is connected to said conductive wiring line.

12. A semiconductor integrated circuit device according to claim 11, wherein said ring oscillation circuits are synchronized to oscillate with said output of each of said ring oscillation circuits being of a substantially identical frequency.

13. A semiconductor integrated circuit device according to claim 12, wherein said ring oscillation circuits are synchronized to oscillate with said output of each of said ring oscillation circuits being of a substantially identical phase.

14. A semiconductor integrated circuit device according to claim 11, wherein said conductive wiring line is formed in a shape of a closed loop.

15. A semiconductor integrated circuit device according to claim 11, wherein said conductive wiring line is formed in a shape of a mesh, and said outputs of at least one inverter of said ring oscillation circuits are connected at intersection points of said mesh.

16. A semiconductor integrated circuit device according to claim 11, wherein said outputs of at least one inverter of said ring oscillation circuits are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said connection points, wherein said interval lengths are substantially equal.

17. A semiconductor integrated circuit device according to claim 11, wherein said outputs of at least one inverter of said ring oscillation circuits are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said connection points, wherein said interval of length is 50 μ m or more.

18. A semiconductor integrated circuit device, comprising:

a plurality of delay lines having multistage connected inverters; and

a conductive wiring line,

wherein an output of at least one inverter of each of said delay lines is connected to said conductive wiring line.

19. A semiconductor integrated circuit device according to claim 18, wherein said delay lines are synchronized to oscillate with the output of each of said inverters being of a substantially identical frequency.

20. A semiconductor integrated circuit device according to claim 19, wherein said delay lines are synchronized to oscillate with the output of each of said inverters being of a substantially identical phase.

21. A semiconductor integrated circuit device according to claim 18, wherein said conductive wiring line is formed in a shape of a closed loop.

22. A semiconductor integrated circuit device according to claim 18, wherein said conductive wiring line is formed in

a shape of a mesh, and said outputs of said at least one inverter of said ring oscillation circuits are connected at intersection points of said mesh.

23. A semiconductor integrated circuit device according to claim 18, wherein said outputs of said at least one inverter of said ring oscillation circuits are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said connection points, wherein said interval lengths are substantially equal.

24. A semiconductor integrated circuit device according to claim 18, wherein said outputs of said at least one inverter of said ring oscillation circuits are connected to said conductive wiring line at connection points with an interval of length of said conductive wiring line between said connection points, wherein said interval of length is 50 μ m or more.

25. A semiconductor integrated circuit device, comprising:

a plurality of circuit blocks having a clock distribution circuit;

a plurality of oscillators, each having an oscillation node and outputting a clock signal from said oscillation node to said clock distribution circuit; and

a conductive wiring connecting said oscillation nodes of each of said oscillators together.

26. A semiconductor integrated circuit device according to claim 25, wherein said oscillators are synchronized to oscillate with a substantially identical frequency at each of said oscillation nodes.

27. A semiconductor integrated circuit device according to claim 26, wherein said oscillators are synchronized to oscillate with a substantially identical phase at each of said oscillation nodes.

28. A semiconductor integrated circuit device according to claim 25, wherein said conductive wiring is formed in a shape of a closed loop.

29. A semiconductor integrated circuit device according to claim 25, wherein said conductive wiring is formed in a shape of a mesh, and said oscillation nodes of said oscillators are connected at intersection points of said mesh.

30. A semiconductor integrated circuit device according to claim 25, wherein said oscillation nodes are connected to said conductive wiring at connection points with an interval of length of said conductive wiring between said connection points, wherein said interval lengths are substantially equal.

31. A semiconductor integrated circuit device according to claim 25, wherein said oscillators are ring oscillation circuits.

32. A semiconductor integrated circuit device according to claim 25, wherein said oscillators are delay lines having multistage connected inverters.

33. A semiconductor integrated circuit device according to claim 25, wherein said circuit blocks comprise a logic circuit or a memory circuit.

34. A semiconductor integrated circuit device, comprising:

a plurality of oscillation circuits;

a wiring connecting each output of said oscillation circuits together;

a plurality of clock distribution circuits that are connected to said oscillation circuits; and

a phase frequency comparator comparing a clock signal of at least one of said clock distribution circuits with a reference clock signal,

wherein said oscillation circuits change oscillation frequency in response to a signal output from said phase frequency comparator.

35. A semiconductor integrated circuit device according to claim 34, wherein said oscillation circuits are synchronized to oscillate with said output of each of said oscillation circuits being of a substantially identical frequency.

36. A semiconductor integrated circuit device according to claim 35, wherein said oscillators are synchronized to oscillate with said output of each of said oscillation circuits being of a substantially identical phase.

37. A semiconductor integrated circuit device according to claim 34, wherein said conductive wiring line is formed in a shape of a closed loop.

38. A semiconductor integrated circuit device according to claim 34, wherein said outputs of said oscillation circuits are connected to said wiring at connection points with an interval of length of said wiring between said connection points, wherein said interval lengths are substantially equal.

39. A semiconductor integrated circuit device according to claim 34, wherein said oscillators are ring oscillation circuits.

40. A semiconductor integrated circuit device according to claim 34, wherein said oscillators are delay lines having multistage connected inverters.

41. A semiconductor integrated circuit device, comprising:

a plurality of oscillators having substantially the same natural oscillation frequency; and

a conductive wiring connecting outputs of each of said oscillators,

whereby all of said oscillators oscillate at substantially said identical frequency independent of fluctuations of a supply of voltage supply to said oscillators.

42. A semiconductor integrated circuit device, comprising:

clock distribution means for distributing clock signals to a plurality of circuit blocks;

a plurality of oscillator means for outputting a clock signal to said clock distribution means; and

means for synchronizing each of an output frequency of said plurality of oscillator means that is independent of fluctuations of supply voltages supplied to said plurality of oscillator means.